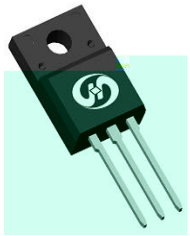
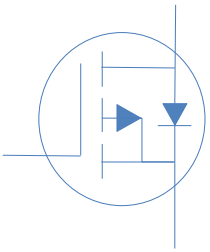
100V P-Ch Power MOSFET

V_{DS}		-100	V
$R_{DS(on),typ}$	V_{GS}=10V	105	mΩ
$I_{D\ (Sillicon\ Limited)}$		-22	A

Part Number	Package	Marking
HTA1K2P10	TO-220F	TA1K2P10





Absolute Maximum Ratings at T_j=25 (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C=25	-22	A
		T_C=100	-15	
Drain to Source Voltage	V_{DS}	-	-100	V
Gate to Source Voltage	V_{GS}	-	±20	V
Pulsed Drain Current	I_{DM}	-	-75	A
Avalanche Energy, Single Pulse	E_{AS}	L=0.1mH, T_C=25	22.5	mJ
Power Dissipation	P_D	T_C=25	38	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to 150	

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	62.5	/W
Thermal Resistance Junction-Case	$R_{\theta JC}$	3.3	/W

Dynamic Characteristics

Input Capacitance	C_{iss}		-	3522	-	
Output Capacitance	C_{oss}	V_{GS}=0V, V_{DS}=-25V, f	nam	130		
			-	114	-	
Total Gate Charge	Q_g		-	58	-	
Gate to Source Charge	Q_{gs}	V_{DD}=-80V, I_D=-11A, V_{GS}=-10V	-	13.8	-	nC
Gate to Drain (Miller) Charge	Q_{gd}		-	10.5	-	
Turn on Delay Time	$t_{d(on)}$		-	15	-	
Rise time	t_r	V_{DD}=-10V, I_D=-1A, V_{GS}=-10V,	-	67	-	ns
Turn off Delay Time	$t_{d(off)}$	R_G=6Ω,	-	50	-	
Fall Time	t_f		-	50	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=-22A	-		1.3	V
Reverse Recovery Time	t_{rr}	I_F=-5A, dI_F/dt=100A/μs	-	150	-	ns
Reverse Recovery Charge	Q_{rr}		-	830	-	nC

Fig 1. Typical Output Characteristics

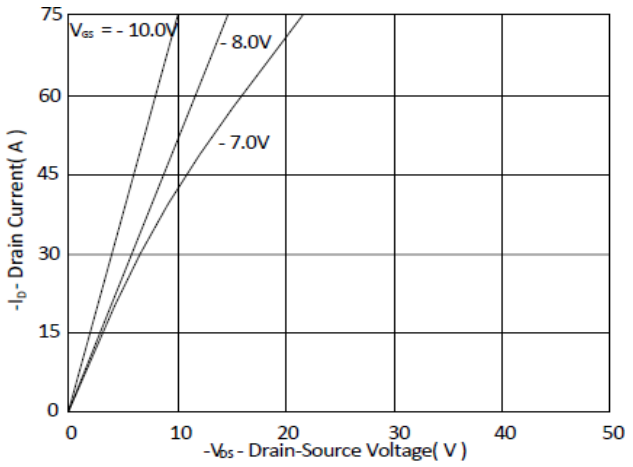


Figure 2. On-Resistance vs. Gate-Source Voltage

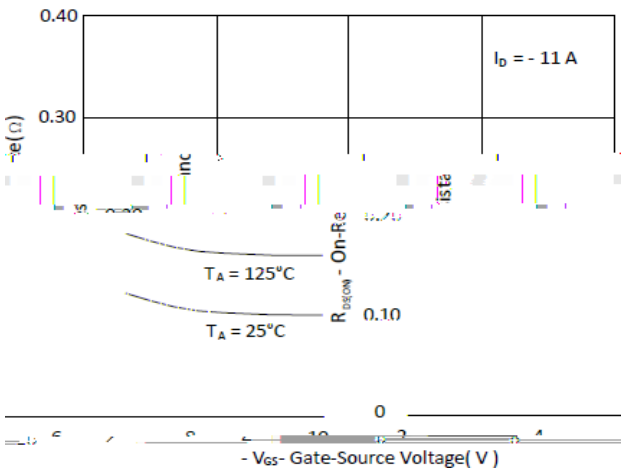


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

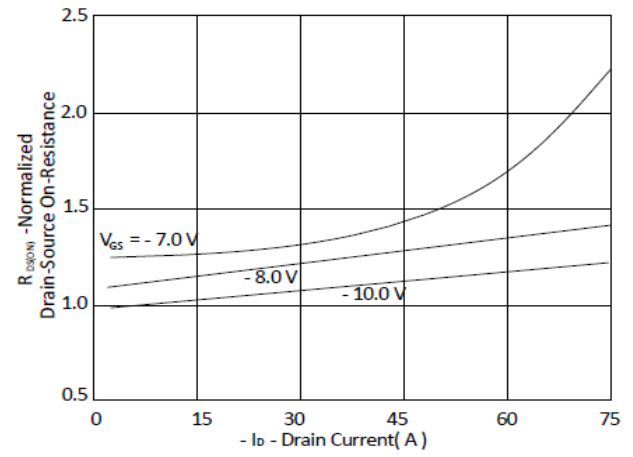


Figure 4. Normalized On-Resistance vs. Junction Temperature

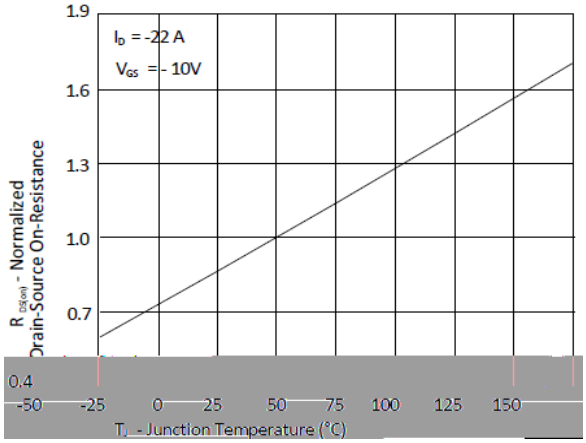


Figure 5. Typical Transfer Characteristics

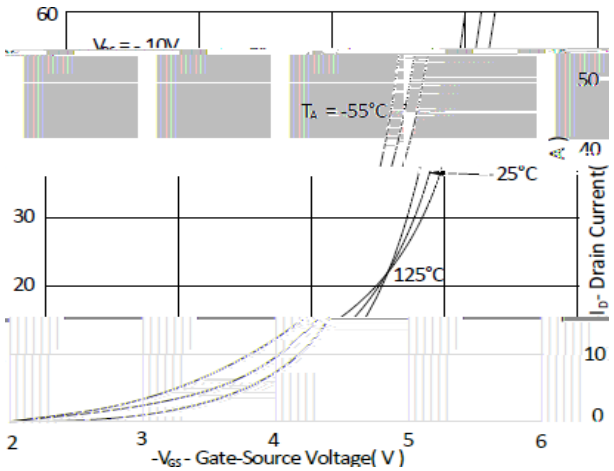


Figure 6. Typical Source-Drain Diode Forward Voltage

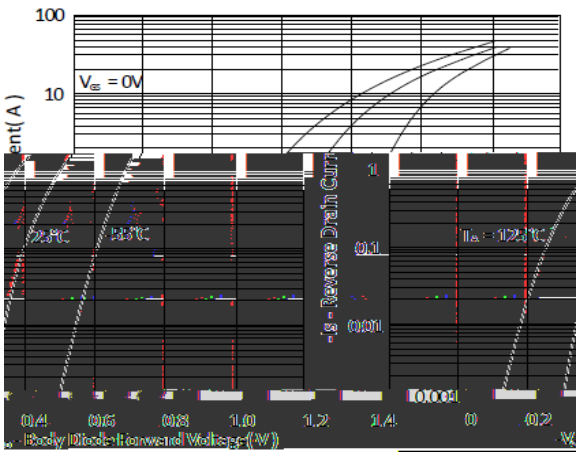


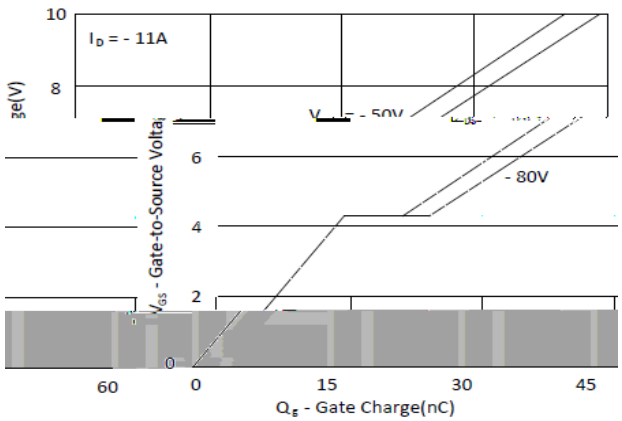
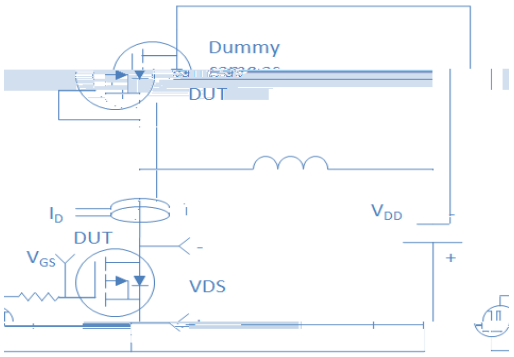
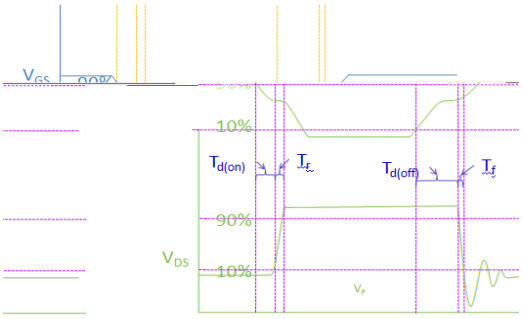
Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage	Figure 8. Typical Capacitance vs. Drain-to-Source Voltage
	

Figure 9. Maximum Safe Operating Area	Figure 10. Single Pulse Maximum Power Dissipation

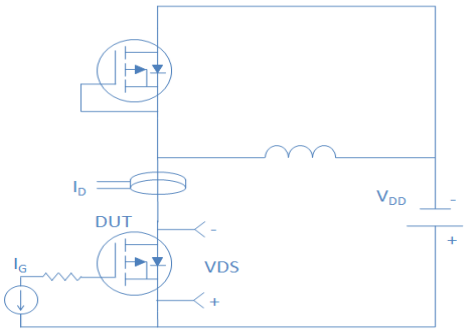
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

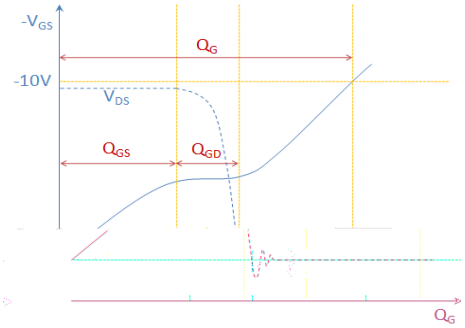
Inductive switching Test



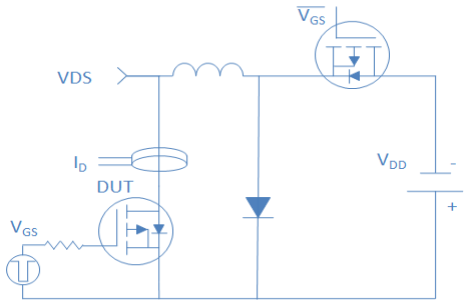


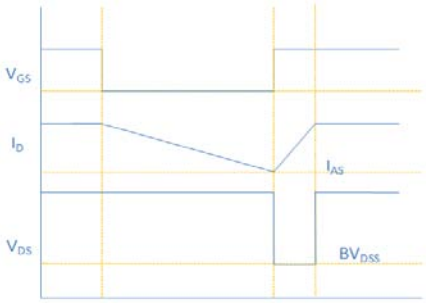
Gate Charge Test



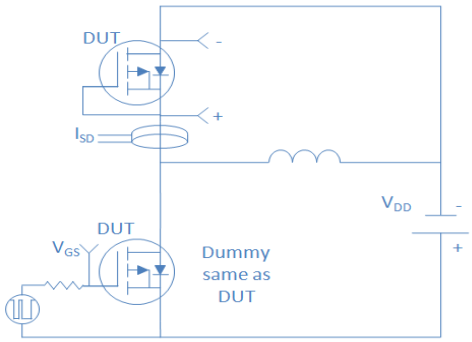


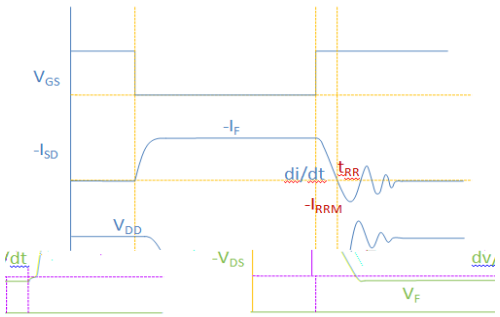
Uclamped Inductive Switching (UIS) Test





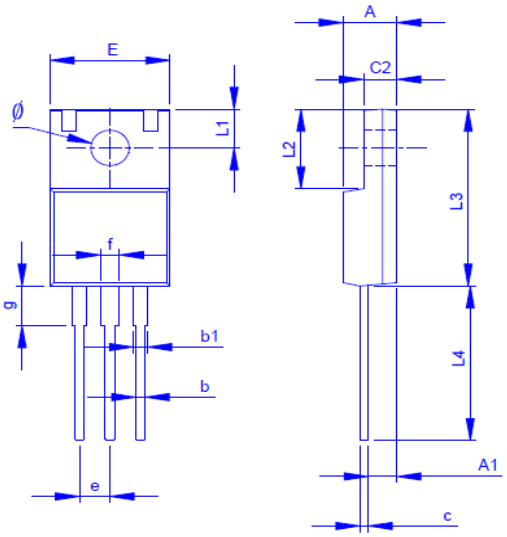
Diode Recovery Test





Package Outline

TO-220F, 3leads



Dimension in mm

Dimension	A	A1	b	b1	c	c2	E	L1	L2	L3	L4	ø	e	f	g
90	4.00	Max.	4.90	2.96	1.05	1.50	0.80	3.20	10.66	3.80	7.50	16.30	14.50	3.50	2.75	1.